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REMARKS

Claims 1-16 were pending before amendment. Claims 1-5 and 7-8 have been cancelled by this amendment without prejudice. Claims 6 has been amended. Claim 6 has been amended to incorporate the elements of cancelled claims 7-8. No new matter has been added. The specification has been amended to correct typographical errors. Reconsideration and allowance of the presently amended application are respectfully requested.

Objection to Specification:

The first paragraph of the specification has been objected to for omitting a reference to the parent application. The paragraph in contention has been amended to include the reference and thus obviates the contention.

The title has been objected to for allegedly being not descriptive. The title has been amended to obviate the contention.

Claim Rejections Under Double Patenting:

Claims 1-16 stand rejected under the judicially created doctrine of obviousness-type double patenting as allegedly being

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unpatentable over claims 1-10 of U.S. Patent No. 6,725,360 to Aldrich et al. ("Aldrich"). Applicant respectfully traverses the double patenting rejections. The present application is a divisional of Applicant's prior Application No. 09/541,116 (now U.S. Patent No. 6,725,360), the same reference relied upon by the Office Action to allege the double patent rejections. The present application is directed to the non-elected claims resulting from the restriction requirement applied by the Office in the parent application, Aldrich, and thus the present application cannot be held as being the same invention as the parent application. Is the Office now admitting that the restriction requirement in Aldrich was improper? The MPEP § 806 states that "Where restriction is required by the Office double patenting cannot be held, and thus, it is imperative the requirement should never be made where related inventions as claimed are not distinct." Also, MPEP § 806.05 adds that "[i]f nondistinct inventions are claimed in separate applications or patents, double patenting must be held, *except where the additional applications were filed consonant with a requirement to restrict in a national application.*" (Emphasis added).

Further, MPEP § 804.01 clearly prohibits certain kinds of double patenting rejections under 35 U.S.C. § 121.

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35 U.S.C. § 121 authorizes the Commissioner to restrict the claims in a patent application to a single invention when independent and distinct inventions are presented for examination. *The third sentence of 35 U.S.C. § 121 prohibits the use of a patent issuing on an application with respect to which a requirement for restriction has been made, or on an application filed as a result of such a requirement, as a reference against any divisional application, if the divisional application is filed before the issuance of the patent. The 35 U.S.C. § 12 prohibition applies only where the Office has made a requirement for restriction.* The prohibition does not apply where the divisional application was voluntarily filed by the applicant and not in response to an Office requirement for restriction. This apparent nullification of double patenting as a ground of rejection or invalidity in such cases imposes a heavy burden on the Office to guard against erroneous requirements for restrictions where the claims define essentially the same invention in different language and which, if acquiesced in, might result in the issuance of several patents for the same invention. (Emphasis added).

If the restriction requirement was correctly applied by the Office in the parent application, Applicant submits that claims 1-16 of the present application are distinctly patentable over the parent application. Further, MPEP § 804.04 requires any double patenting rejections relying upon a parent application, where a restriction requirement was enforced, must be approved by the Technology Director before mailing. Applicant did not find any evidence to indicate that the Technology Center Director approved the double patenting rejections.

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§ 804.04 Submission to Technology Center Director

In order to promote uniform practice, every Office action containing a rejection on the ground of double patenting which relies on the parent application rejecting the claims in a divisional or continuing application where the divisional or continuing application was filed because of a requirement to restrict made by the examiner under 35 U.S.C. § 121, including a requirement to elect species, must be submitted to the Technology Center Director for approval prior to mailing. If the rejection on the ground of double patenting is disapproved, it shall not be mailed but other appropriate action shall be taken. Note MPEP § 1003.

For at least these reasons, claims 1-16 are not properly rejected based on double patenting over Aldrich.

Claim Rejections Under 35 U.S.C. § 102 (e)

Claims 1-16 stand rejected as allegedly being anticipated by U.S. Patent No. 6,092,094 to Ireton ("Ireton"). These contentions are respectfully traversed.

Claims 1-5 have been cancelled without prejudice and thus obviates the contentions with respect to claims 1-5.

Claim 6

Although Ireton teaches processing multiple independent narrow width operands, the number of independent operands and the data size are specified by the encoded instruction (col. 7, line 51-53) and the control unit 46. Ireton's control unit 46

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asserts a control signal, and in response to the control signals, "adder circuit 50 and multiplication circuit 54 interprets the 32 bits...as one 32 bit operand, two 16 bit operands, four 8 bit operands, or eight 4 bit operands" (col. 7, lines 58-63). In other words, the multiplication circuit 54 is instructed to process the 32 bit data as narrower width operands using individual multiplier circuits 90 as shown in FIG. 5. Therefore, the individual multipliers circuits are not configured after determining the size of the data, but rather are configured strictly based on the instructions and the control signal from the control unit 46. Thus, Ireton does not teach configuring the multiplier into the first structure of a single n -bit multiplier when the data is greater than $(n/2)$ -bits and configuring the multiplier into the second structure of two $(n/2)$ -bit multiplier when the data is $(n/2)$ -bits or less as required in claim 6.

The multiplier circuits 54 in Ireton multiply "four bit portions of the first and second operands, forming eight bit results (or products)...a portion of the product of the first and second operands is computed" (col. 10, lines 43-49). Thus, Ireton teaches that in response to the control signal from the control unit 46, multiplier circuit 54 takes the x -bit portion

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of the first operand and x-bit portion of the second operand based on the encoded instruction and the control signal. For example, if the instruction calls for 8 bit operation, the lower 8 bit portions of first and second operands are multiplied together. Applicant submits that this is not the same as *configuring the multiplier into the first structure of a single n-bit multiplier when the data is greater than (n/2)-bits and configuring the multiplier into the second structure of two (n/2)-bit multiplier when the data is (n/2)-bits or less* as required in claim 6.

For at least these reasons, claim 6 is allowable over Ireton.

Claims 9-11

Claims 9-11 are dependent upon claim 6 and thus are patentable over Ireton for at least the reasons as stated above for claim 6 above.

In addition, Ireton fails to teach a *plurality of arithmetic logic units to collect the processed data* as recited in claim 9. Ireton teaches collecting the results from the adder circuit 50 and the multiplier circuit 54 using the multiplexor circuit 56, but does not specify the components of the multiplexor circuit 56 (col. 7, lines 25-27 and FIG. 2), and

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thus fails to teach or suggest a plurality of arithmetic logic units as recited in claim 9. Ireton also fails to teach *a flop which stores the result of the multiplier* as recited in claim 10 and *at least one arithmetic logic unit which adds the result from the multiplier to a running total* as recited in claim 11. In Ireton, the control unit 46 sends a selection line 58 to the multiplexor circuit 56 holding the results, whereby a result is selected and transmitted to a plurality of result bus 26 (col. 7, lines 25-31 and FIG. 2). Ireton does not disclose a flop for storing the results or a arithmetic logic unit for adding to a running total as recited in claims 9-11.

For at least these additional reasons, claims 9-11 are patentable over Ireton.

Claim 12

Claim 12: A method comprising:
determining a size of data to be processed;
configuring a first processing path for data of
n-bits if the data size is greater than (n/m)-bits;
and
dividing the first processing path into multiple
processing paths *if the data size is (n/m)-bits or less.*

In contrast to claim 1, Ireton teaches using execution units 20 to execute instructions specifying wide operands and single instruction multiple data (SIMD) instructions specifying multiple narrow operands. (col. 4, lines 8-11). Integer

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operation circuits of the execution units 20 are configured to interpret the operands either as single values of particular width or as multiple independent values of narrower widths depending on the instructions (col. 4, lines 11-17). Thus, Ireton does not **determine a size of the data** to be processed as recited in claim 1. Rather, Ireton's execute instructions specifies interpretation of the size of the operand.

For example, if the integer operation circuits are configured to operate upon 32 bit operands and the particular SIMD instruction specifies 4 bit operands, then eight independent values from each operand are operated upon and eight independent results are produced. (col. 4, lines 25-29).

While the integer operator circuits can process the operands in parallel as multiple independent values having narrow widths, the SIMD instruction limits all values to the same integer operation, either a multiplier or an adder (col. 4, lines 14-17). Ireton teaches a first processing path, an adder, and a second processing path, a multiplier, independent of the data size. The integer operator circuits are configured as an adder or a multiplier based on the execution instruction (col. 7, lines 10-47), and independent of the size of the data. The size of the data is selected by the execution instructions and corresponding operands of specific data size are recalled from

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memory and sent to the first processing path including an adder or a second processing path including a multiplier.

Thus, the size of the data is selected by Ireton's execution instructions and corresponding operands of specific data size are recalled from memory and sent to the first processing path including an adder or a second processing path including a multiplier. Ireton does not teach or suggest configuring and dividing the first processing path based on the determined data size as recited in claim 12.

For at least this reason, claim 12 is patentable over Ireton.

Claims 13-16

Claims 13-16 depend from claim 12 and thus are patentable over Ireton for at least reasons stated for claim 12 above.

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CONCLUSION

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue, or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Claims 1-2, 4-6, and 9-16 are in condition for allowance, and a notice to that effect is respectfully solicited.

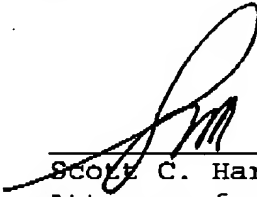
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No fees are believed due with this response. Please
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06-1050, referencing the attorney docket number shown above.

Respectfully submitted,

Date: October 6, 2005



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